Aarush Assudani

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Education

Georgia Institute of Technology | Atlanta, GA *Expected Graduation, May 2027*
Bachelor of Science in Computer Engineering, GPA 3.91

Skills

Digital Design & RTL: Verilog, VHDL, SystemVerilog, RTL design, testbenches, UVM, SVA, FSM, MMIO, AXI4-Lite
FPGA & Hardware: AMD Xilinx Zynq, Intel Cyclone V FPGA (DE10), ESP32, Raspberry Pi, PCB design (Altium)
VLSI & EDA Tools: Cadence Xcelium/Innovus, Quartus Prime, Vivado, ModelSim, TCL, YoSys HQ
Embedded & Testing: Oscilloscopes, logic analyzers, FreeRTOS, PlatformIO, ESP-IDF
Programming & Systems: C/C++ (Firmware), Python, Java, RISC-V/MIPS assembly, Bash, Git, Linux
Communication: Design proposals, technical reports, instruction manuals, presentations

Work Experience

Center for Research into Novel Compute Hierarchies | Atlanta, GA *Jan. 2026 - Present*
RTL Design & Verification Engineer

- Targeting 0.34 cycles/byte for XChaCha20 cryptography algorithm on AMD Xilinx Zynq UltraScale+ MPSoC, 30–47x faster than the ARM Cortex-A53 software baseline
- Designed the RTL core around 4 parallel ARX quarter-round cells with HChaCha20 subkey derivation which hits 2.33 Gbps at 100 MHz in 22 clock cycles per 64-byte block, using 4–7% of LUTs with no BRAM or DSP
- Wrote 50+ SVA assertions across 10 modules in YoSys HQ, formally proving encryption/decryption correctness

TerraSense | Atlanta, GA *May 2025 - Present*
Embedded Systems Engineer / Startup

- Co-founded TerraSense which was accepted into Georgia Tech Create-X and demoed at Launch Demo Day
- Prototyping a sensory substitution insole on breadboard with a FSR pressure array, ESP32-C6, TENS stimulation circuit, and 3D-printed insole housing while targeting an alternative to existing $900+ systems
- Wrote multi-threaded C++ firmware on ESP32-C6 to keep sensory polling, BLE transmission, and TENS feedback from interfering. Stress-tested under real walking conditions using a logic analyzer and UART logs

Georgia Tech Student Government Association | Atlanta, GA *Aug. 2025 - Present*
Software Engineering Intern / Joint Financial Data Committee

- Automated fund request processing in Python that handles 800+ annual requests from 600+ student organizations managing $10M in university disbursements that cut manual review time by 90%
- Added an anomaly detection layer to flag unusual patterns in historical transaction data, improving how the finance team catches errors before audit

Projects

Body-Mounted Accessible Game Controller | ESP32, MPU-6050, ElevenLabs STT Spring 2026

- Built with a 3-person team and demoed at a hackathon: a body-mounted controller that straps to any limb, letting people with limited or no hand motor control play any game (tested on Elden Ring, Forza, and Hades)
- Wrote ESP32 firmware for the MPU-6050 IMU with on-the-fly switching between analog and discrete control modes; designed a custom 3D-printed Velcro enclosure for universal body attachment
- Hooked in ElevenLabs STT so the entire experience, launching games, remapping controls, adjusting settings, runs on voice commands with no physical UI needed

SCOMP 16-bit Processor | VHDL, Quartus Prime Spring 2025

- Extended a 15-instruction RISC ISA to 20 instructions (SUB, JPOS, JNZ) in VHDL on Intel Cyclone V FPGA, with full fetch-decode-execute pipeline and MMIO across an 11-bit address bus
- Added a custom arithmetic coprocessor with hardware multiply, divide, and modulus with dedicated registers for overflow and divide-by-zero detection